WHAT IS CLAIMED IS:

1. A system for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a forward fast Fourier transform (FFT) unit calculating a forward fast Fourier transform (FFT) from the data;

a complex multiplication unit receiving the FFT-processed data and calculating a spatial derivative in the frequency domain from the FFT-processed data;

an inverse fast Fourier transform (IFFT) unit converting the spatial derivative in the frequency domain from the complex multiplication unit into the time domain; and

a computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from the IFFT unit.

2. A system as recited in claim 1, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\frac{\partial H_c}{\partial b} + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

3. A system as recited in claim 1, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

4. A system as recited in claim 1, wherein the FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

5. A system as recited in claim 4, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

6. A system for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a plurality of forward fast Fourier transform (FFT) units, each FFT unit calculating a forward fast Fourier transform (FFT) from the data;

a plurality of complex multiplication units, each complex multiplication unit receiving the FFT-processed data from a corresponding FFT unit and calculating a spatial derivative in the frequency domain from the FFT-processed data;

a plurality of inverse fast Fourier transform (IFFT) units, each IFFT unit converting the spatial derivative in the frequency domain from a corresponding complex multiplication unit into the time domain; and

a plurality of computation engines, each computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from a corresponding IFFT unit.

7. A system as recited in claim 6, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\frac{\partial H_c}{\partial b} + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

8. A system as recited in claim 6, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

9. A system as recited in claim 6, wherein the plurality of FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

10. A system as recited in claim 9, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

11. A computer hardware configuration for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a forward fast Fourier transform (FFT) unit calculating a forward fast Fourier transform (FFT) from the data;

a complex multiplication unit receiving the FFT-processed data and calculating a spatial derivative in the frequency domain from the FFT-processed data;

an inverse fast Fourier transform (IFFT) unit converting the spatial derivative in the frequency domain from the complex multiplication unit into the time domain; and

a computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from the IFFT unit.

12. A computer hardware configuration as recited in claim 11, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\frac{\partial H_c}{\partial b} + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

13. A computer hardware configuration as recited in claim 11, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

14. A computer hardware configuration as recited in claim 11, wherein the FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

15. A computer hardware configuration as recited in claim 14, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

16. A computer hardware configuration for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a plurality of forward fast Fourier transform (FFT) units, each FFT unit calculating a forward fast Fourier transform (FFT) from the data;

a plurality of complex multiplication units, each complex multiplication unit receiving the FFT-processed data from a corresponding FFT unit and calculating a spatial derivative in the frequency domain from the FFT-processed data;

a plurality of inverse fast Fourier transform (IFFT) units, each IFFT unit converting the spatial derivative in the frequency domain from a corresponding complex multiplication unit into the time domain; and

a plurality of computation engines, each computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from a corresponding IFFT unit.

17. A computer hardware configuration as recited in claim 16, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\frac{\partial H_c}{\partial b} + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

18. A computer hardware configuration as recited in claim 16, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

19. A computer hardware configuration as recited in claim 16, wherein the plurality of FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

20. A computer hardware configuration as recited in claim 19, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.